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Controllable doping and wrap-around contacts to electrolessly etched silicon nanowire arrays

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Abstract

Top-down electroless chemical etching enables non-lithographic patterning of wafer-scale nanostructured arrays, but the etching on highly doped wafers produces porous structures. The lack of defect-free nanostructures at desired doping and the difficulties in forming reliable electrical side-contacts to the nanostructure arrays limits their integration into high performance nanoelectronics. We developed a barrier layer diffusion technique to controllably dope wafer-scale silicon nanowire arrays (10^{17}–10^{20} cm^{-3}) produced by chemically etching lightly doped silicon wafers. In order to achieve low resistance top-side electrical contacts to the arrays, we developed a two step tip-doping procedure to locally dope the tips ($\sim 10^{20}$ cm^{-3}) to metallic levels. The dopant concentration is characterized by depth profiling using secondary ion mass spectroscopy and four-point probe electrical measurements. Further, array scale electrical measurements show that the tip-doping lowers the specific contact resistivity ($\sim 10^{-5}$ Ω cm^2) since the metallic tips enable direct tunneling of electrons across the nickel silicide contacts to the nanowire arrays. This work provides a scalable and cost-effective doping approach to control charge injection and charge conduction in nanowire arrays, thus advancing their integration into various device applications.

Keywords: silicon nanowire arrays, metal assisted chemical etching, electrical contacts

(Some figures may appear in colour only in the online journal)

1. Introduction

High density integration of functional nanomaterials at large scales will enable the transition of nanoscale research into real-world applications. Large scale integration of one-dimensional nanostructures into vertical arrays and thin-films is already enabling high performance technologies in photovoltaics [1–4], nanoelectronics [5, 6], bio-sensing [7, 8], battery anodes [9–12] and thermoelectrics [13]. There is considerable interest in generating wafer-scale nanostructure arrays using non-lithographic patterning techniques to provide a scalable and cost-effective implementation of nanoscale device technologies. A fabrication scheme of particular interest is the top-down electrochemical etching technique that produces vertically aligned nanostructure arrays on bulk wafers [14, 15]. We previously demonstrated the metal-assisted chemical etching (MACE) conjugated with self-assembled metallic templates can generate wafer-scale silicon nanowire arrays with wire densities up to 40% [16]. However, the morphology of the nanowires generated by the electrochemical etching techniques depends on the doping concentration of the starting wafer. It is widely reported that MACE on highly doped Si wafers produces porous structures [17–19]. The lack of defect-free nanostructures at optimal doping limits the application of electrochemically etched nanostructures in nanoelectronics. Thus, it is imperative to

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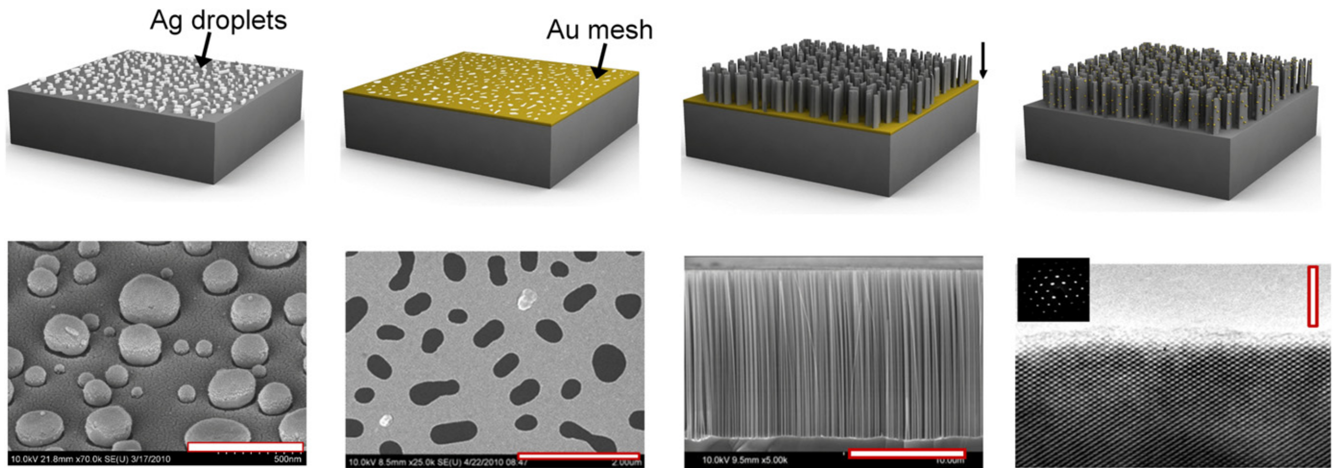

Figure 1. (a) Thermal dewetting pattern of silver droplets after annealing 10 nm Ag film for 350 °C for 4 h. (b) The gold mesh fabricated by Ag lift off serves as the pattern for subsequent etching. (c) Etching in the solution of HF and H_2O_2 produces vertically aligned nanowire array. (d) The HRTEM image and the selected area diffraction pattern reveals the NWs obtained are single crystalline. The scale bars represent a length of (a) 500 nm, (b) 2 μm, (c) 10 μm, (d) 2 nm.

develop a rapid, repeatable and scalable approach to controllably dope array-scale vertical nanostructures integrated on the parent substrate.

Another important limitation in integrating the nanostructure arrays into high performance electronics is the challenge to form low-resistance metallic contacts to the top of arrays [20]. In vertically aligned nanowire arrays, the deposited metal wraps around the tips of the arrays to form electrical contacts. The charge injection efficiency through the metal-semiconductor interface can potentially limit device performance and impose scaling limits on the devices. Charge injection at metal-semiconductor interface occurs across a length scale called the transfer length, L_T. The transfer length scales as $(\rho_c/\rho_w)^{1/2}$ where ρ_c is the specific contact resistivity and ρ_w is the intrinsic resistivity of the device [20]. If the electrical contact length at the tips (L_C) is less than the transfer length, then current crowding at the contact increases the contact resistance (R_c) rapidly as $\coth(L_c/L_T)$. Current crowding negatively impacts device efficiencies due to undesired joule heating at contacts. For example, the efficiency of a thermoelectric generator module [21] can drop by an order in magnitude for an order increase in R_c. In several applications, the availability of wire tips for forming electrical contacts is only several hundreds of nanometers while the transfer length is typically a few micrometers. Current crowding effects can be minimized in these situations by increasing the doping at the tips to as high as $N \sim 10^{20}$ cm^{-3} (for Si) to reduce L_T below 1 μm. High doping at the contact also prevents carrier depletion in the nanowire tips by reducing the depletion width, $W \propto 1/\sqrt{N}$. Since metallic doping levels cannot be extended into the device, we require strategies to selectively dope the tips degenerately without affecting doping in the rest of the array.

In this Letter, we present an approach to controllably dope the nanowire arrays fabricated by MACE on Si substrate and characterize the resultant dopant profiles using secondary ion mass spectroscopy (SIMS). We further develop a two-step tip doping approach that creates metallic doping levels (10^{20} cm^{-3}) locally at the array tips while the remainder of the wires maintain as-etched doping concentration. We characterize our doping approaches by conducting two-point and four-point probe electrical measurements of the post-doped nanowires. Finally, we study contact resistivity in nickel wrap-around contacts to p-type SiNW arrays and investigate charge transport mechanism across the tip contacts. Although several recent works have investigated the electron transport mechanisms in wrap-around contacts for individual NWs [22–24], the present study is distinct in providing insights into the behavior at an array-scale that is technologically relevant.

2. Nanowire array fabrication and *ex situ* doping

We use MACE to obtain wafer-scale arrays of silicon nanowires (SiNWs). The details of the fabrication steps can be found in our recent publication [16], but the important steps are described here. The process begins with the deposition of thin Ag film on a lightly doped p-Si wafer ($\rho \sim 1$–$5\,\Omega$ cm). Annealing at 350 °C for 4 h under 4×10^{-7} torr thermally dewets the Ag into spherical particles (contact angle >90°) on the surface (figure 1(a)). The inverse pattern of the Ag particles is formed by deposition of ~10 nm Au and subsequent liftoff of Ag in NH_4OH (32%):H_2O_2 (30%) solution (figure 1(b)). The Au mesh pattern now serves as a template for the metal-assisted chemical etch (MACE) in an aqueous solution of HF (49%):H_2O_2 (30%): ethanol = 13:2:19 (v : v : v). The highly anisotropic MacEtch (figure 1(c)) catalyzed at Au-Si interface etches Si substrate into nanowires arrays 500 nm–1200 nm in length (~0.6 μm min^{-1} etch rate). Aqua regia etch for 90 s removes the Au mesh. The as-synthesized NW arrays are generally smooth (RMS roughness ~0.5 nm) with areal fractions ~30–40%. Analysis of the wire array using scanning electron microscopy (SEM) reveal a tight distribution in the NW lengths with standard deviations

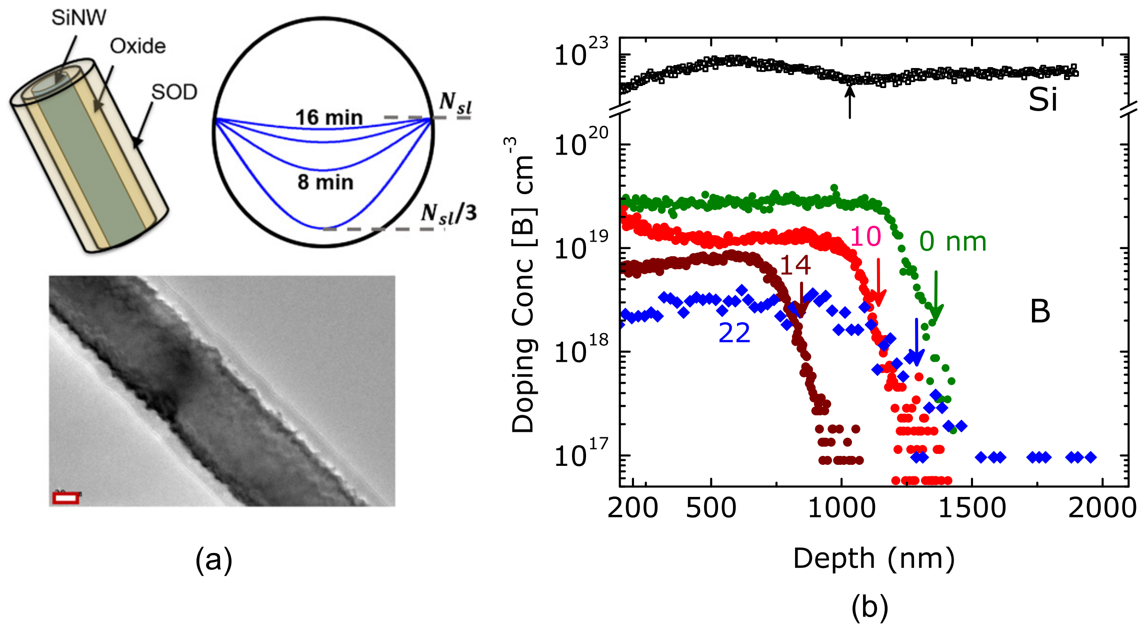

Figure 2. (a) Schematic of barrier layer doping using spin-on dopants with TEM micrograph of barrier oxide layer formed on the nanowire surface. The dopant concentration profiles relative to solid-solubility limit (N_{sl}) in the nanowire cross-section (~100 nm diameter) for doping times in steps of 4 min. The scale bar is 20 nm. (b) The SIMS depth profile of the boron-doped nanowire arrays, doped with PECVD barrier layer of thickness labeled against each profile. The arrows represent the length of the NW array measured from SEM before the profiling.

$\Delta L \sim 12\%$ within a given array. Nanowires assume the non-circular cross-section of the initial Ag particles, as illustrated in figure 1(c) with the average characteristic diameter of 120–140 nm and eccentricity ~0.5. Transmission electron micrographs (TEM) confirmed that the nanowires obtained by etching are solid single-crystalline nanowires [25] (figure 1(d)).

We previously reported that metal assisted chemical etching of degenerately doped silicon wafers generates mesoporous nanowires [17]. Porosity can be detrimental in various device applications and thus a controllable and scalable doping approach is needed. Ion implantation of dopants into the highly dense and high aspect ratio NW arrays cannot achieve uniform doping across NW cross-section. monolayer doping (MLD) is an attractive way to controllably inject dopant atoms into Si lattice up to tens of nanometer depth [26, 27]. MLD techniques require growth of self-assembled dopant-containing monolayer on crystalline SiNW surfaces and the subsequent rapid thermal annealing enables diffusion of dopants from the surface to the NW lattice. But, it has been reported that electrochemically etched nanostructures possess amorphized surfaces [15] which complicates the surface chemistry of monolayer assembly on MACE NWs. We instead use solid source diffusion of dopants which has been successfully used for achieving conducting NW arrays [28, 29]. This technique is used to dope solid NWs initially obtained from MACE on low-doped substrate using spin-on dopants (SODs) in an *ex situ* manner.

The doping concentration and the uniformity of dopant profiles in solid source diffusion process is affected by choice of annealing time and temperature. We achieve the control of doping concentration by a technique called barrier layer doping. Before the SODs contact the arrays, we form thin oxide layer on the sidewalls of NWs, either by thermal oxidation or plasma enhanced CVD. The oxide layer acts as a barrier to dopant diffusion and thus by varying its thickness (<25 nm), we can control the dopant concentration in the NWs. The surface oxide layer further protects the nanowire sidewalls from the organic contaminants. In our doping scheme, the oxide thickness serves as the control parameter for dopant concentration at a constant annealing temperature and time. We spin the SODs on the NW arrays with the oxide layer at 3000 rpm for 30 s and then bake at 270 C for 10 min The dopant diffusion is activated by annealing the samples at 950 C for 15 min, called the pre-deposition step. We use SODs of boron or phosphorus (Borofilm or phosphorofilm from Filmtronics©) to dope the NW arrays to p- or n-type polarities respectively. A short BOE etch removes the borosilicate/phosphorosilicate glass formed as a part of annealing. Finally, we drive-in the dopants at 975 C for another 10 min.

The pre-deposition/drive-in temperature and annealing time are chosen appropriately so that the dopants are uniformly distributed across the cross-section of the NWs. Modeling or measuring dopant diffusion into a nanowire is challenging, but the temperature-time condition that ensures complete radial penetration of dopant can be readily obtained by solving the diffusion equation. For a Si nanowire covered by spin-on dopant, the concentration of the dopant at the nanowire surface is fixed to the solid-solubility limit of dopant species (N_{sl}) at the pre-deposition temperature. In a cylindrical wire of radius r_0, the time dependent dopant concentration $N(r, t)$ in the cross-section of the NW is given

by [30]

$$\frac{N(r,t)}{N_{sl}} = 1-2\sum_{k=1}^{\infty}\frac{J_0\left[\lambda_k(r/r_0)\right]}{\lambda_k J_1(\lambda_k)}\exp\left(-\frac{D\lambda_k^2}{r_0^2}t\right),$$

where D is dopant diffusivity in silicon at temperature T, λ_k is the kth zero of the Bessel function J_0. Figure 2(a) shows the doping concentration profiles in the cross-section of a ~100 nm wire in steps of $t = 4$ min We find the pre-deposition of dopant at 950 C over 15 min yields uniform doping concentrations across the cross-section of a nanowire.

Variation in doping along the length of the nanowires is characterized by SIMS. The primary ion beam for dopant depth profiling is either Cs^+ or O_2^- for phosphorus (n-type) and boron (p-type) doped wires respectively. A standard ion-implanted sample of known dose is also measured at the same alignment conditions to extract relative scaling factor (RSF) for the dopant species. We convert the etching time to depth by measuring the final crater depth using profilometry and assuming the sputtering rate to be constant. Figure 2(b) shows the SIMS concentration depth profiles for p-type nanowire arrays, doped with several thickness of barrier oxide layer. We observe that doping is uniform across the length of the nanowires and that the dopant concentration decreases with increase in oxide layer thickness. The depths at which there is a sharp decline in the SIMS profile match well with the lengths of nanowires estimated using SEM. Thus, varying the thickness of the oxide barrier layer in the range 1 nm–22 nm, we can controllably dope the nanowires in the doping concentration from 2×10^{19} cm^{-3} to 4×10^{18} cm^{-3} as shown in figure 2(b). We obtain phosphorus doped NW arrays with the dopant concentration ~10^{20} cm^{-3} without a barrier layer and 6×10^{19} cm^{-3} with 10 nm oxide using this procedure.

3. Selective doping of nanowire arrays at metal-semiconductor interface

Forming reliable electrical contacts to the nanowire arrays for all doping levels is especially challenging due to the current crowding and carrier depletion effects. Efficient charge injection across metal-nanowire interface requires a strategy to locally dope the sections of the nanowire arrays that contact the metal to relatively high doping. We achieve the selective doping, referred to as tip doping, using a two-step process using spin-on glass (SOG) and SOD. Initially, the nanowire arrays are filled with SOG by spinning SOG at 2000 rpm for 30 s. The SOG is baked on hot plate at 110 C and 270 C for 90 s at each step. The SOG is then cured in nitrogen environment for 1 h at 350 C. The initial thickness of SOG layer is usually 1.5 μm for the conditions described above. We then etch the SOG using Freon gas (CF_4) by reactive ion etching (RIE) till the SOG thickness typically ~100 nm below the tip of the nanowires. The dry etching also etches Si at a rate (20 nm min) that is half that of SOG (40 nm min). Figure 3(a) shows a SEM image of nanowire tips exposed in the SOG filled NW array of length 850 nm. We find that the nanowire tips assume conical shape due to partial etching of Si by RIE.

A layer of SOD is now spun on the SOG-filled NW arrays such that dopant solution only contacts the NW tips exposed post-RIE. We follow the same steps of doping described in the previous section, but the doping time is now reduced to less than 5 min at 950 C. The short doping times ensures the tip of the NW array is doped without affecting the doping in the rest of the wires. The section of wires covered by SOG is not doped in this process. We remove the SOG layer after doping by 2 min etch in 49% HF. We conducted dopant depth profile analysis of NW arrays using SIMS. Figure 3(b) shows the SIMS depth profiles of NWs (of length 850 nm) doped at the tips by boron at different annealing times. For this analysis, we expose ~150 nm of NW tips for doping. For samples with annealing times >3 min, we observe undesirable diffusion of the dopants from the tips to the rest of the NWs. Using the depth to which dopants diffuse into the rest of the array as a function of annealing time, we estimate the axial diffusion constant D of boron to be ~4×10^{-14} cm^2 s^{-1} in our SiNW samples at 950 C (inset of figure 3(b)). The observed diffusion constant is higher than that in bulk Si (6×10^{-15} cm^2 s^{-1}) and we expect surface defects of NWs and the elastic strain in the NW core may contribute to enhanced diffusivity in our NWs [31]. Based on this calculation, an annealing time of about 2 min should confine the dopants within the tips. At short annealing times, the dopant diffusion is shallow in the NW cross-section with dopants only present within the diffusion length $L \sim \sqrt{Dt}$ from the NW surface ($L = 20$ nm for $t = 2$ min). Since the dopant atom count obtained in SIMS is averaged over the areal cross-section of the several wires, the average dopant distribution profile appears to decrease with depth in shallow doped conical sections as shown in figure 3(b).

4. Electrical measurements of arrays and single nanowires

We have measured the electrical properties of the nanowire arrays to verify the success of the post-doping and the tip-doping processes, and compared the results against SIMS characterization. Electrical measurements of the NWs provide an alternate characterization of the carrier concentration in the NWs post-doping. The array-scale electrical measurements can only be two-point probe (2pp) between isolated top-side contacts. Since it is difficult to extract nanowire array resistance from that at the contacts in 2pp measurements, we conducted four-point probe (4pp) electrical measurements on individual nanowires extracted from the array.

4.1. Single nanowire resistivity measurements

We start with dispersing the nanowires from the array onto an oxidized Si substrate (200 nm thermal oxide). The wires are then located by SEM in order to draw an e-beam pattern for the four electrical pads over the NW. Before e-beam lithography to define the pads, we deposit ~30 nm PECVD oxide film to protect the NW surface from the organic contaminants. The oxide film also provides surface passivation minimizing

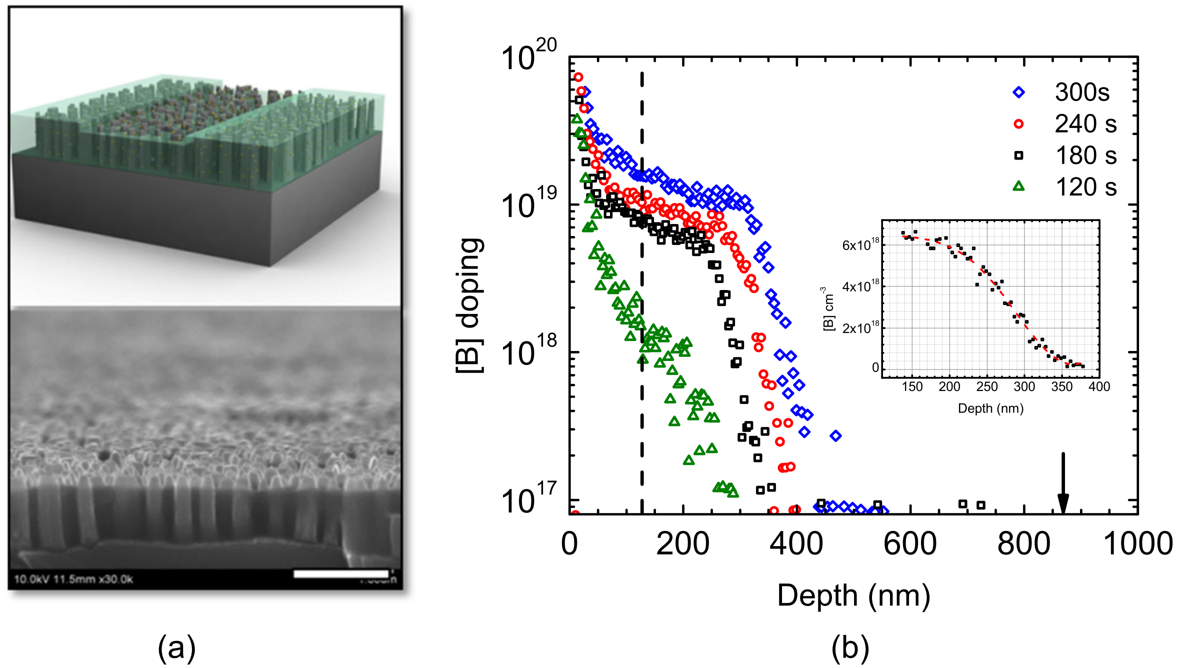

Figure 3. (a) NW arrays filled by spin-on glass and etched down locally to expose the tips of nanowires of ~150 nm. The scale bar is 1 μm. (b) SIMS depth profiles of tip-doped NWs of lengths 850 nm for different doping times. (Inset shows the dopant profile in linear scale for 240 s doping time used to extract boron diffusivity in the NW array.)

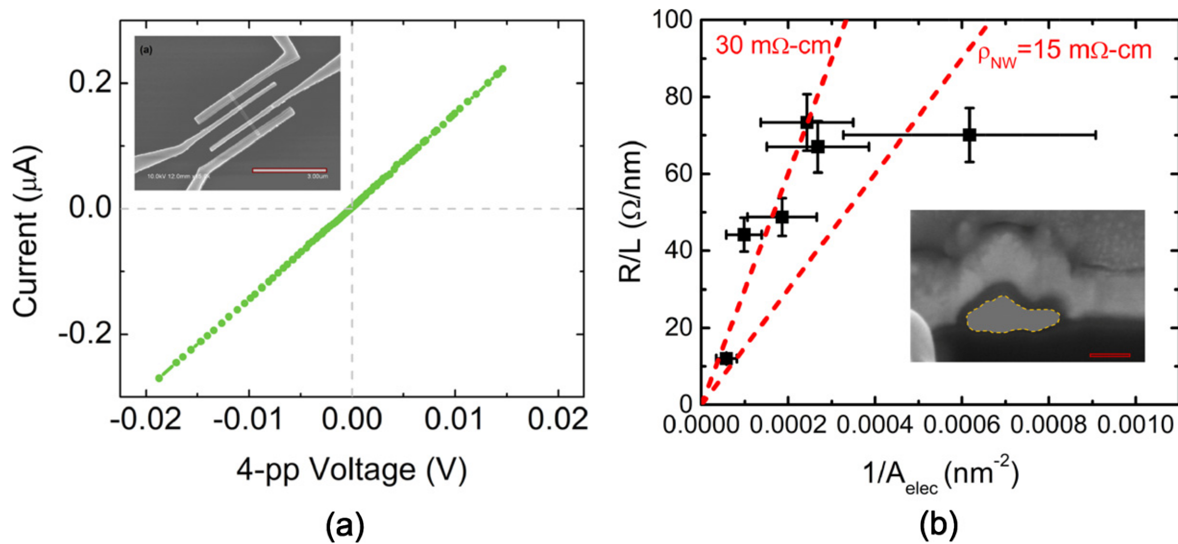

Figure 4. (a) Four point probe *I–V* measurements of a single nanowires from the doped array. (b) The 4pp resistance values for various wires with different diameters from an array doped to $\sim 10^{19}$ cm^{-3}, as measured by SIMS. Inset shows the FIB cross-section of the nanowire with scale bar of 100 nm.

the carrier depletion at the NW surface. We deposit Ni (130 nm)/Au (30 nm) for electrical pads and the subsequent RTP at 320 °C for 3 min provides Ohmic contacts. The measurement platform and the 4pp *I–V* measurements of a single NW are shown in figure 4(a).

We extract the nanowire resistivity $\rho_w = (V/I)\ A_{nw}/L_{eff}$ where the cross-section A_{nw} is calculated from SEM diameter of the wire and L_{eff} considers the total length of nanowire between and under the metallic contacts [22]. Figure 4(b) relates the electrical resistance of six nanowires extracted from the same array with their cross-section. We find the *ex situ* doping reduces the electrical resistivity of SiNWs by over three orders down to 15–30 mΩ cm. The SIMS data for the NW array used in figure 4(b) shows dopant concentration ranging from 8×10^{18}–10^{19} cm^{-3} across the depth. The measured resistivity values are within a factor of two to four in comparison with bulk Si at this doping. Previous electrical measurements in the literature also show an increase in resistivity in nanowire compared to bulk, mainly arising from the carrier depletion effects at nanowire surface [32–34]. Carrier depletion at surfaces reduces the effective cross-section of NWs contributing to electrical conduction. In such

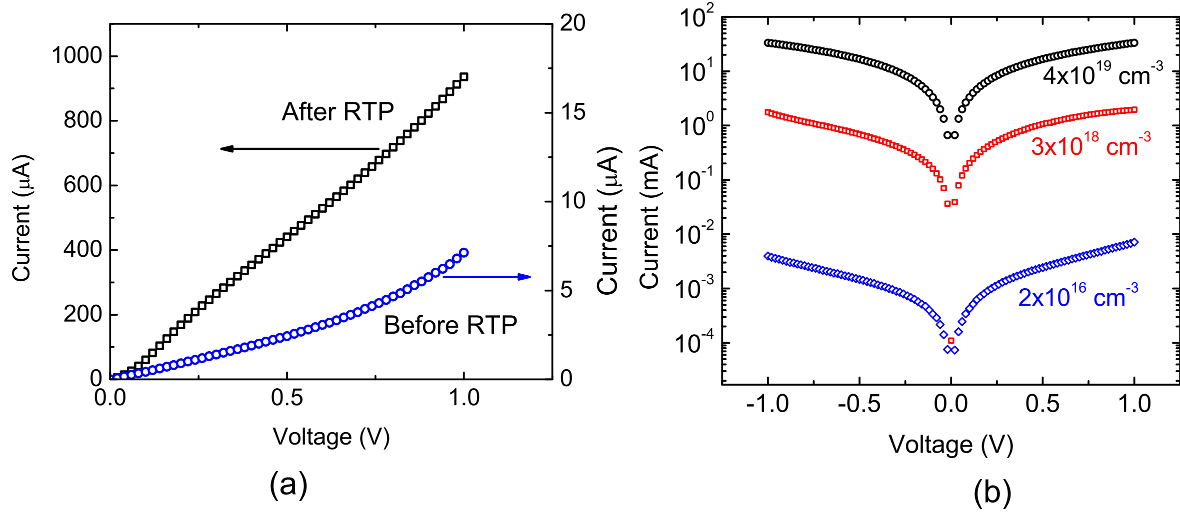

Figure 5. (a) Contact resistance of Ni-SiNW array (10^{18} cm^{-3}) contacts before and after the rapid thermal annealing. (b) The 2pp *I–V* measurements for specific contact resistivity of Ni contacts with SiNW arrays at different doping levels.

case, the resistivity of NWs is obtained by considering electrical radius of NWs rather than physical radius obtained from SEM [35]. In our wires, calculating the area of active conduction channel is quite challenging due to non-circular cross-section of the NWs. The nanowires in our work have non-circular cross-section since they assume the shape of thermally dewetted silver droplets, used as template for MACE. The inset in figure 4(b) shows the focused ion beam cross-section of a nanowire. However, at doping levels of $\sim 10^{19}$ cm^{-3}, we expect the depletion thickness is within 5–8 nm and thus we expect that this effect alone cannot explain the apparent increase in resistivity. Previous reports of MACE nanostructures report that chemical etching introduces moderate porosity or point defects in the structures which cannot be captured by HR-TEM. Non-circular cross-section also present high curvature surfaces that can lead to compressive strain in NWs, which can affect the carrier mobility in NWs.

4.2. Resistivity measurements of wrap-around contacts

We conducted two point probe electrical measurements of the NW arrays to verify the success of tip doping. In order to facilitate electrical contacts to the arrays, a smooth surface is created on top of the array by filling the wire array with SOG. We etch SOG such that nanowire tips of $L_c \sim 100$ nm are exposed for metallic contacts. We deposit nickel pads (thickness of 200 nm) as the electrical contacts on SOG filled NW arrays. The Ni contacts are then annealed at 320 C by rapid thermal processing (RTP) for 3 min to facilitate ohmic contacts. We choose low annealing temperature of 320 C to ensure negligible diffusion of NiSi into the SiNWs [36]. Figure 5(a) shows that the silicidation of Ni contacts by RTP improves the electrical contact conductance by ~100x for the 10^{18} cm^{-3} doped array. Figure 5(b) shows the *I–V* curves of NW array samples with different tip-doping concentrations. The lengths, diameters and the areal coverage of the nanowires is consistent among the NW arrays. The measured 2pp resistance (R) has contribution from the contact resistance ($2R_c$), the parent substrate and the nanowire array. By choosing nanowire array lengths $\sim 1\,\mu$m and electrical pad sizes $100 \times 100\,\mu$m^2, the electrical resistance from the nanowire arrays contributes less than 3% to the total resistance R. The substrate resistance is determined in a separate TLM measurement is 30 Ω for all the NW samples. From figure 5(b), we conclude that the extracted contact resistance R_c of Ni wrap-around contacts to the NW arrays decreases by over three orders as the tips are doped to degenerate levels.

To calculate the specific contact resistivity, we use the TLM theory developed for planar contacts [24]. In this theory, the contact resistance in the current crowding regime ($L_c < L_T$) is expressed as $R_c = \rho_w L_T / A \coth(L_c/L_T)$ where ρ_w is the resistivity of NW with cross-sectional area A, the transfer length $L_T = \sqrt{2r\rho_c/3\rho_w}$ and ρ_c is the specific contact resistivity. The nanowire resistivity ρ_w is obtained by 4pp measurement and SIMS data. We observe that the tip doping decreases ρ_c by a factor of 4×10^2 at 3×10^{18} cm^{-3} and 6×10^3 at 4×10^{19} cm^{-3} in comparison to low-doped NW arrays without tip doping. The exact value of specific contact resistivity is difficult to extract due to uncertainty in calculating total wrap-around area of the metal to the conical tips of the array. Assuming that the metal wraps around all the exposed nanowire tips, we get an upper bound for contact resistivity of $13 \times 10^{-2}\,\Omega$ cm^2 for 2×10^{16} cm^{-3}, $3.5 \times 10^{-4}\,\Omega$ cm^2 for 3×10^{18} cm^{-3} and $2.2 \times 10^{-5}\,\Omega$ cm^2 for 4×10^{19} cm^{-3} doping respectively. The decreasing trend of ρ_c with doping indicates that the charge transport across metal-NW transitions from thermionic emission to direct tunneling at high doping. In the event of direct tunneling of carriers across nickel silicide contacts, the specific contact resistivity can be obtained from the field emission (FE) theory of electron transport. For FE transport [37, 38], $\rho_c \propto \exp\left(2\Phi_b \sqrt{\varepsilon m^*/N}\right)$, where Φ_b is the barrier height of Ni–Si interface, ε is the permittivity, m^* is the hole effective mass and N is the carrier concentration in

NWs at the contact. In a separate measurement, we extract the barrier height at Ni silicide contacts to the low doped p-type NW array to be ~0.41 V. We use an approximation for N to be equal to the doping concentration measured from SIMS. Now using the above relation, we find that the observed decrease in specific contact resistivity with doping in our experiments agrees well with FE theory.

5. Summary

MACE procedures on degenerately doped wafers produce porous nanostructures, severely limiting their application in nanoelectronics. In this paper, we present controllable doping techniques that enables efficient charge injection and charge transport in MACE generated nanostructures at array-scale. The solid crystalline silicon nanowires obtained by MACE on lightly doped Si wafer are doped *ex situ* through a barrier layer to doping concentrations in the range of 10^{17}–10^{19} cm^{-3}. The low-resistance electrical contacts to the doped arrays requires the nanowire sections at the metallic contacts to be highly degenerate without affecting the doping in rest of the array. To achieve this, we introduce a two-step procedure using SOD to dope the nanowire tips locally in the arrays filled with SOG. Nanowire doping and tip-doping techniques are characterized by SIMS using depth profiling. Electrical measurements of the nanowire arrays further provided an alternate way to evaluate the doping procedures, and are compared against the SIMS studies. We find the electrical resistivity of the nanowires decreases by three-orders upon doping and the values are within a factor of four of the bulk resistivity at doping concentration obtained by SIMS. We also study the behavior of the nickel silicide contacts to the boron doped nanowire arrays across various tip-doping concentrations. The sharp decline of the specific contact resistivity down to $\sim 2 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ at 4×10^{19} cm^{-3} is in accordance with the field emission theory, indicating the direct tunneling of charge carriers at metal-nanowire interfaces. The results shown in this paper advances the integration of MACE structures in wide span of device applications in photovoltaics, thermoelectrics and nanoelectronic devices.

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